[0346] The first interlayer insulating layer **180** may include an upper portion **180***b* including an element semiconductor material, and a lower portion **180***a* not including an element semiconductor material.

[0347] Referring to FIG. **30**, the first and the second dummy gate electrodes **120***p*, **220***p* and the first and the second dummy gate insulating layers **125***p*, **225***p* may be removed.

[0348] As a result, the first trench **121** defined by the first gate spacers **131**, **132**, and the second trench **221** defined by the second gate spacers **231**, **232** may be formed.

[0349] Referring to FIG. **31**, the first gate electrode **120** filling the first trench **121** and the second trench **221** may be formed.

[0350] FIG. **32** is a block diagram of an SoC system comprising a semiconductor device according to an example embodiment.

[0351] Referring to FIG. **32**, the SoC system **1000** includes an application processor **1001** and a dynamic random-access memory (DRAM) **1060**.

[0352] The application processor **1001** may include a central processing unit (CPU) **1010**, a multimedia system **1020**, a bus **1030**, a memory system **1040** and a peripheral circuit **1050**.

[0353] The CPU **1010** may perform arithmetic operation necessary for driving of the SoC system **1000**. In some example embodiments, the CPU **1010** may be configured on a multi-core environment which includes a plurality of cores.

[0354] The multimedia system **1020** may be used for performing a variety of multimedia functions on the SoC system **1000**. Such multimedia system **1020** may include a three-dimensional (3D) engine module, a video codec, a display system, a camera system, a post-processor, and so on.

[0355] The bus **1030** may be used for exchanging data communication among the CPU **1010**, the multimedia system **1020**, the memory system **1040** and the peripheral circuit **1050**. In some example embodiments, the bus **1030** may have a multi-layer structure. For example, an example of the bus **1030** may be a multi-layer advanced high-performance bus (AHB), or a multi-layer advanced eXtensible interface (AXI), although example embodiments are not limited herein.

[0356] The memory system **1040** may provide environments for the application processor **1001** to connect to an external memory (e.g., DRAM **1060**) and perform high-speed operation. In some example embodiments, the memory system **1040** may include a separate controller (e.g., DRAM controller) to control an external memory (e.g., DRAM **1060**).

[0357] The peripheral circuit **1050** may provide environments for the SoC system **1000** to have a seamless connection to an external device (e.g., main board). Accordingly, the peripheral circuit **1050** may include a variety of interfaces to allow compatible operation with the external device connected to the SoC system **1000**.

[0358] The DRAM **1060** may function as an operation memory necessary for the operation of the application processor **1001**. In some example embodiments, the DRAM **1060** may be arranged externally to the application processor **1001**, as illustrated. For example, the DRAM **1060** may be packaged into a package on package (PoP) type with the application processor **1001**.

[0359] At least one of the above-mentioned components of the SoC system **1000** may include at least one of the semiconductor devices according to the example embodiments explained above.

[0360] In concluding the detailed description, those skilled in the art will appreciate that many variations and modifications can be made to the example embodiments without substantially departing from the principles of the present inventive concepts. Therefore, the disclosed preferred example embodiments of the inventive concepts are used in a generic and descriptive sense only and not for purposes of limitation.

1. A semiconductor device, comprising:
- a gate spacer on a substrate, the gate spacer defining a trench;
- a gate electrode filling the trench; and
- an interlayer insulating layer on the substrate, the interlayer insulating layer surrounding the gate spacer, the interlayer insulating layer including a first portion having germanium.

2. The semiconductor device of claim **1**, wherein a width of the trench is substantially same with increasing distance from the substrate.

3. The semiconductor device of claim **1**, wherein a width of the trench decreases with increasing distance from the substrate.

4. The semiconductor device of claim **3**, wherein
- the gate electrode includes a first sidewall and a second sidewall opposed to each other, and
- the first sidewall of the gate electrode and the second sidewall of the gate electrode have slopes at an acute angle with a bottom surface of the gate electrode.

5. The semiconductor device of claim **1**, wherein
- the gate electrode includes a first sidewall and a second sidewall opposed to each other,
- the first sidewall of the gate electrode has a slope at a right angle with a bottom surface of the gate electrode, and
- the second sidewall of the gate electrode has a slope at an acute angle with the bottom surface of the gate electrode.

6. The semiconductor device of claim **1**, wherein the interlayer insulating layer comprises a second portion which does not include the germanium.

7. The semiconductor device of claim **6**, wherein
- the interlayer insulating layer includes a lower portion and an upper portion,
- the upper portion of the interlayer insulating layer includes the first portion of the interlayer insulating layer, and
- the lower portion of the interlayer insulating layer includes the second portion of the interlayer insulating layer, the second portion not including the germanium.

8. The semiconductor device of claim **1**, wherein a concentration of the germanium in the first portion of the interlayer insulating layer increases with increasing distance from the substrate.

9. The semiconductor device of claim **1**, wherein an upper surface of the interlayer insulating layer and an upper surface of the gate electrode are positioned at a same plane.

10.-**33**. (canceled)